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06/10/2004

HAYES, SOLOWAY P.C.
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Kim Good	(Depositor's name)
<i>Kim Good</i>	(Signature)
September 1, 2004	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,995	08/27/2003	Susumu Takano	NEC OSP-9770 DIV II	4368

TITLE OF INVENTION: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING LOGIC CIRCUIT COMPRISING TRANSISTORS WITH LOWER THRESHOLD VOLTAGE VALUES AND IMPROVED PATTERN LAYOUT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	09/10/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DON P	2819	326-121000

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1 HAYES SOLOWAY P.C.

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Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☒ corporation or other private group entity ☐ government

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Henry Soloway 9/1/04

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